

[0218] Each of the plurality of driving stages SRC1' to SRCn' and the dummy driving stage SRC(n+1)' includes an output terminal OUT, a carry terminal CR, an input terminal IN, a control terminal CT, a clock terminal CK, a first ground terminal V1, a second ground terminal V2, and a bias voltage terminal VB.

[0219] The output terminal OUT of each of the plurality of driving stages SRC1' to SRCn' is connected to a corresponding gate line among the plurality of gate lines GL1 to GLn. Gate signals generated from the plurality of driving stages SRC1' to SRCn' are provided to the plurality of gate lines GL1 to GLn through the respective output terminals OUT.

[0220] The carry terminal CR of each of the plurality of driving stages SRC1' to SRCn' is electrically connected to an input terminal IN of the next driving stage thereof. The carry terminals CR of the plurality of driving stages SRC1' to SRCn' respectively output carry signals.

[0221] The input terminal IN of each of the plurality of driving stages SRC2' to SRCn' and the dummy driving stage SRC(n+1)' receives the carry signal of the previous driving stage thereof. In one exemplary embodiment, for example, the input terminal IN of the third driving stages SRC3' receives a carry signal of the second driving stage SRC2'. The input terminal IN of the first driving stage SRC1' receives the start signal STV that starts driving of the gate driving circuit 100' instead.

[0222] The control terminal CT of each of the plurality of driving stages SRC1' to SRCn' is electrically connected to the carry terminal CR of the next driving stage thereof, and receives the carry signal of the next driving stage thereof.

[0223] In one exemplary embodiment, for example, the control terminal CT of the second driving stage SRC2' receives a carry signal output from the carry terminal CR of the third driving stage SRC3'. In an alternative exemplary embodiment, the control terminal CT of each of the plurality of driving stages SRC1' to SRCn' may be electrically connected to the output terminal OUT of the next driving stage thereof.

[0224] The control terminal CT of the driving stage SRCn' disposed at the end receives a carry signal output from the carry terminal CR of the dummy driving stage SRC(n+1)'. The control terminal CT of the dummy driving stage SRC(n+1)' receives the start signal STV.

[0225] The clock terminal CK of each of the plurality of driving stages SRC1' to SRCn' and the dummy driving stage SRC(n+1)' receives one of the first clock signal CKV and the second clock signal CKVB. Among the plurality of driving stages SRC1' to SRCn', clock terminals CK of odd-numbered driving stages SRC1' and SRC3' may respectively receive the first clock signal CKV. Among the plurality of driving stages SRC1' to SRCn', clock terminals CK of even-numbered driving stages SRC2' and SRCn' may respectively receive the second clock signal CKVB, where n is an even number. The first clock signal CKV and the second clock signal CKVB may have different phases from each other.

[0226] The first ground terminals V1 of the plurality of driving stages SRC1' to SRCn' and the dummy driving stage SRC(n+1)' receive the first ground voltage VSS1. The second ground terminals V2 of the plurality of driving stages SRC1' to SRCn' and the dummy driving stage SRC(n+1)' respectively receive the second ground voltage VSS2. The first ground voltage VSS1 and the second ground voltage VSS2 have different voltage levels from each other, and

second ground voltage VSS2 has a voltage level that is lower than that of the first ground voltage VSS1.

[0227] The bias voltage terminals VB of the plurality of driving stages SRC1' to SRCn' and the dummy driving stage SRC(n+1)' receive the back bias voltage VBB.

[0228] Next, an exemplary embodiment of a driving stage of FIG. 14 will be described in detail with reference to FIG. 15.

[0229] FIG. 15 shows a circuit diagram of an exemplary embodiment of a driving stage of FIG. 14.

[0230] FIG. 15 illustrates an exemplary embodiment of an i-th driving stage SRCi'1 (here, i is a positive integer) among the plurality of driving stages SRC1' to SRCn' shown in FIG. 14. Each of the plurality of driving stages SRC1' to SRCn' of FIG. 14 may have the same circuit structure as the i-th driving stage SRCi'1.

[0231] Referring to FIG. 15, an exemplary embodiment of the i-th driving stage SRCi'1 includes output units 710-1 and 710-2, a controller 720, an inverter 730, pull-down units 740-1 and 740-2, and holding units 750-1 and 750-2.

[0232] The output unit 710-1 outputs an i-th gate signal, and the output unit 710-2 outputs an i-th carry signal.

[0233] The pull-down unit 740-1 pulls down the output terminal OUT to the first ground voltage VSS1 connected to the first ground terminal V1. The pull-down unit 740-2 pulls down the carry terminal CR to the second ground voltage VSS2 connected to the second ground terminal V2.

[0234] The holding unit 750-1 maintains the output terminal OUT in the pulled-down state. The holding unit 750-2 maintains the carry terminal CR in the pulled-down state.

[0235] The controller 720 controls operation of the output units 710-1 and 710-2, the pull-down units 740-1 and 740-2, and the holding units 750-1 and 750-2.

[0236] Hereinafter, the configuration of the i-th driving stage SRCi'1 will be described in greater detail.

[0237] In an exemplary embodiment, the output unit 710-1 includes a first output transistor T1. The first output transistor T1 includes an input end connected to the clock terminal CK, a control end connected to the first node Q, and an output end that outputs the i-th gate signal.

[0238] The output unit 710-2 includes a second output transistor T15. The second output transistor T15 includes an input end connected to the clock terminal CK, a first control end connected to the first node Q, an output end that outputs an i-th carry signal, and a second control end connected to the carry terminal CR.

[0239] As shown in FIG. 14, clock terminals CK of some (SRC1', SRC3', and SRCn-1') of the driving stages SRC1' to SRCn' and the dummy driving stage SRC(n+1)' receive the first clock signal CKV. Clock terminals CK of the remaining driving stages (SRC2', SRC4', . . . , and SRCn') of the driving stages SRC1' to SRCn' receive the second clock signal CKVB. The first clock signal CKV and the second clock signal CKVB are complimentary signals. In an exemplary embodiment, the first clock signal CKV and the second clock signal CKVB may have a phase difference of about 180°.

[0240] The controller 720 turns on the first output transistor T1 and the second output transistor T15 in response to an (i-1)-th carry signal received through the input terminal IN from the previous driving stage.

[0241] The controller 720 turns off the first output transistor T1 and the second output transistor T15 in response to an (i+1)-th carry signal received through the control terminal